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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,123	08/28/2001	Gurtej Singh Sandhu	303.676US3	6644

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

NC

Office Action Summary	Application No.	Applicant(s)
	09/941,123	SANDHU ET AL.
	Examiner	Art Unit
	Johannes P Mondt	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46,47 and 57-82* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46,47 and 57-82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The examiner has considered all items listed in the Information Disclosure Statement filed 8/28/01 and entered as Paper No. 2.

Claim Objections

1. ***Claims 68 and 81*** are objected to because of the following informalities: "borophosphous silicate glass" (lines 7 and 8-9 in claim 68, and lines 7 and 9 in claim 81) should be replaced by "borophosphosilicate glass". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. ***Claims 60, 62 – 64, 66, 68, and 70*** are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al (5,239,196).

With regard to claim 60: Ikeda et al teach (cf. Figures 4, 6, 7, and 9) a memory device (cf. abstract, first sentence), comprising:

a semiconductor substrate 1 (cf. column 33, lines 34-38);

a memory array MAY coupled to the semiconductor substrate (cf. Figure 2 and column 28, lines 60-62);

a control circuit CC operatively coupled to the memory array MB (said operative coupling is inherent for any control circuit to function) (cf. Figure 2 and column 29, lines 2-3);

an I/O circuit (cf. Figures 6 and 7), operatively coupled to the memory array (said operative coupling is inherent for any input to get into the memory array or output to be retrieved from it) (cf. column 60, lines 49-59);

an electronic device (MISFET Q_{t1}) (cf. column 36, line 20 – column 38, line 8) coupled to the semiconductor substrate (cf. Figure 9), the electronic device having an active region (channel forming region within the p well region 2 within the semiconductor substrate 1; see column 36, lines 34-36);

an insulator 27 (cf. Figure 9 and column 53, lines 53-59) over the active region;

an alloy layer of titanium alloy $TiSi_x$ (cf. column 36, lines 55-59) within a contact opening 28 (cf. Figure 9 and column 61, lines 57-59) in the insulating layer 27, the contact opening being at least partially over the active region (see Figure 9) (this aspect is inherent in MISFET devices, as it simply implies that the gate, which, as we will see, is positioned within the contact opening, is at least partially over the active region);

since $TiSi_x$ is both a titanium alloy and titanium silicide, the final limitation of this claim is automatically met by arbitrarily splitting the $TiSi_x$ gate material into two portions that are in contact with each other, and calling said portions titanium silicon alloy and titanium silicide, respectively.

In conclusion, Ikeda et al anticipate claim 60.

With regard to claim 62: the insulator 27 includes SiO_2 (cf. column 53, lines 53-59).

With regard to claim 63: the memory device of claim 60 as anticipated by Ikeda et al includes a transistor Q_{t1} (cf. column 36, line 20 – column 38, line 8).

With regard to claim 64: Ikeda et al teach (cf. Figures 4, 6, 7, and 9) a memory device (cf. abstract, first sentence), comprising:

a semiconductor substrate 1 (cf. column 33, lines 34-38);

a memory array MAY coupled to the semiconductor substrate (cf. Figure 2 and column 28, lines 60-62);

a control circuit CC operatively coupled to the memory array MB (said operative coupling is inherent for any control circuit to function) (cf. Figure 2 and column 29, lines 2-3);

an I/O circuit (cf. Figures 6 and 7), operatively coupled to the memory array (said operative coupling is inherent for any input to get into the memory array or output to be retrieved from it) (cf. column 60, lines 49-59);

a transistor (MISFET Q_{t1}) (cf. column 36, line 20 – column 38, line 8) formed on the semiconductor substrate (cf. Figure 9), the transistor having a source/drain region 18 (cf. column 36, line 67 – column 37, line 3);

an insulator layer 27 (cf. Figure 9 and column 53, lines 53-59) over the source/drain region;

an alloy layer of titanium alloy $TiSi_x$ (cf. column 36, lines 55-59) within a contact opening 28 (cf. Figure 9 and column 61, lines 57-59) in the insulating layer 27, the contact opening being at least partially over the source/drain region (see Figure 9) (this aspect is inherent in MISFET devices, as it simply implies that the channel region is appropriately influenced by the gate, which, as we will see, is positioned within the contact opening);

since $TiSi_x$ is both a titanium alloy and titanium silicide, the final limitation of this claim is automatically met by arbitrarily splitting the $TiSi_x$ gate material into two portions that are in contact with each other, and calling said portions titanium silicon alloy and titanium silicide, respectively.

In conclusion, Ikeda et al anticipate claim 64.

With regard to claim 66: the insulator layer 27 includes SiO_2 (cf. column 53, lines 53-59).

With regard to claim 68: Ikeda et al teach (cf. Figures 4, 6, 7, and 9) a memory device (cf. abstract, first sentence), comprising:

a semiconductor substrate 1 (cf. column 33, lines 34-38);

a memory array MAY coupled to the semiconductor substrate (cf. Figure 2 and column 28, lines 60-62);

a control circuit CC operatively coupled to the memory array MB (said operative coupling is inherent for any control circuit to function) (cf. Figure 2 and column 29, lines 2-3);

an I/O circuit (cf. Figures 6 and 7), operatively coupled to the memory array (said operative coupling is inherent for any input to get into the memory array or output to be retrieved from it) (cf. column 60, lines 49-59);

an electronic device (MISFET Q_{t1}) (cf. column 36, line 20 – column 38, line 8) formed on the semiconductor substrate (cf. Figure 9), the electronic device having an active region (cf. column 36, line 67 – column 37, line 3);

a borophosphosilicate glass layer 27 (cf. Figure 9 and column 53, lines 53-59) over the active region;

an alloy layer of titanium alloy $TiSi_x$ (cf. column 36, lines 55-59) within a contact opening 28 (cf. Figure 9 and column 61, lines 57-59) in the insulating layer 27, the contact opening being at least partially over the active region (see Figure 9) (this aspect is inherent in MISFET devices, as it simply implies that the channel region is appropriately influenced by the gate, which, as we will see, is positioned within the contact opening);

since $TiSi_x$ is both a titanium alloy and titanium silicide, the final limitation of this claim is automatically met by arbitrarily splitting the $TiSi_x$ gate material into two portions that are in contact with each other, and calling said portions titanium silicon alloy and titanium silicide, respectively.

In conclusion, Ikeda et al anticipate claim 68.

With regard to claim 70: the memory device of claim 68 as anticipated by Ikeda et al includes a transistor (MISFET Q_{t1}) (cf. column 36, line 20 – column 38, line 8).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claims 67, 71-72, 74-77, and 79-81*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al (5,239,196), in view of Xu et al (6,217,721 B1).

With regard to claim 67: As detailed above, Ikeda et al anticipate claim 64. Ikeda et al do not necessarily anticipate the further limitation defined by claim 67. However, it is common knowledge in the art of the fabrication of semiconductor integrated circuit devices, including memory devices, that, as the density of elements on an integrated circuit increases, the width of contacts, vias, or trenches, and other apertures must decrease while due to a minimum dielectric thickness needed for insulation their depth cannot decrease correspondingly; and that for the resulting high-aspect-ratio contact holes, for instance of the order of 2, or even 5 or greater, physical vapor deposition (PVD) is particularly useful for filling the high-aspect-ratio with aluminum, which is well-known to be the preferred filling material, and wets well to titanium to form a titanium alloy, while the bottom part of the titanium film is silicided, as evidenced by Xu et al (cf. title, abstract, column 2, lines 3-13, column 4, lines 34-35, and column 8, lines 23-35, and column 26, lines 9-12). The teaching in this regard by Xu et al is combinable with the invention taught by Ikeda et al, as increased density would improve the efficiency and integrability of the invention of Ikeda et al. The inventions can be combined,

because only the well-known common goal of increasing memory array density is involved; nothing except the width of the contact hole needs to be changed, while Xu et al exactly teaches how to cope with the fabrication technology aspects of this change, and hence expectation of success is reasonable. The motivation is obviously greater device capability per square inch.

With regard to claims 71 and 77: As detailed above, Ikeda et al anticipate claim 64. Ikeda et al do not necessarily anticipate the further limitation of high-aspect ratio of the contact opening as defined in claim 77. However, it is common knowledge in the art of the fabrication of semiconductor integrated circuit devices, including memory devices, that, as the density of elements on an integrated circuit increases, the width of contacts, vias, or trenches, and other apertures must decrease while due to a minimum dielectric thickness needed for insulation their depth cannot decrease correspondingly; and that for the resulting high-aspect-ratio contact holes, for instance of the order of 2, or even 5 or greater, physical vapor deposition (PVD) is particularly useful for filling the high-aspect-ratio with aluminum, which is well-known to be the preferred filling material, and wets well to titanium to form a titanium alloy, while the bottom part of the titanium film is silicided, as evidenced by Xu et al (cf. title, abstract, column 2, lines 3-13, column 4, lines 34-35, and column 8, lines 23-35, and column 26, lines 9-12). The teaching in this regard by Xu et al is combinable with the invention taught by Ikeda et al, as increased density would improve the efficiency and integrability of the invention of Ikeda et al. The inventions can be combined, because only the well-known common goal of increasing memory array density is involved; nothing except the width of the contact hole needs to

be changed, while Xu et al exactly teaches how to cope with the fabrication technology aspects of this change, and hence expectation of success is reasonable. The motivation is obviously greater device capability per square inch.

With regard to claim 72: this claim is different only from claim 60 (anticipated by Ikeda et al) through the further limitation that the aspect ratio of the contact hole should be large. The above-detailed comment in connexion with claim 67 thus is pertinent to render, given the teaching by Ikeda et al, the claim obvious in view of Xu et al.

With regard to claim 74: the memory device of claim 68 as anticipated by Ikeda et al includes a transistor (MISFET Q_{t1}) (cf. column 36, line 20 – column 38, line 8).

With regard to claim 75: the insulator layer 27 includes SiO_2 (cf. column 53, lines 53-59).

With regard to claim 76: insulator layer 27 includes a borophosphosilicate glass layer 27 (cf. Figure 9 and column 53, lines 53-59).

With regard to claim 79: the insulator layer 27 includes SiO_2 (cf. column 53, lines 53-59).

With regard to claim 80: insulator layer 27 includes a borophosphosilicate glass layer 27 (cf. Figure 9 and column 53, lines 53-59).

With regard to claim 81: this claim combines all limitations of claims 77 and claim 80, and none other. Please be referred to the discussion of the rejections of claims 77 and 80.

6. ***Claim 46*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al (5,239,196).

The only limitation in claim 46 that is extraneous to the limitations defined by claim 60 is that the memory array, control circuit and I/O circuit *each* contain the layer of titanium alloy and titanium silicide contact as defined by claim 60, which Ikeda et al does not necessarily teach. However, because Ikeda et al teach the memory array to comprise transistors (Q_t), the control circuit to comprise transistors (Q_d), and the flip-flop circuit as data storage and retrieval unit (input/output circuit) to comprise both drive and transfer transistors (cf. column 1, line 11-39), and because a replacement of the polysilicide gate 7 for Q_d by titanium silicide as implemented for gate 13 of the transfer transistors would improve the response time of said gate 7 through an increase in the electrical conductivity of said gate 7 (the examiner takes official notice that metal conducts better than polysilicon), it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the abovementioned extraneous limitation.

7. ***Claims 57-59*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al (5,239,196), in view of Xu et al (6,217,721 B1). Ikeda et al teach (as discussed above) a memory device, comprising a memory array, a control circuit operatively coupled to the memory array, and an I/O circuit operatively coupled to the memory array; wherein at least one of the memory array, control circuit and I/O circuit comprises a contact opening or via or contact having a titanium alloy layer formed in a contact hole and a titanium silicide layer formed overlying a silicon base layer. Ikeda et al do not necessarily teach (a) said silicon base layer to be exposed, nor do Ikeda et al necessarily teach (b) said titanium alloy layer to be formed overlying the walls of the

contact hole, (c) and a fill coupled to the titanium alloy layer comprising of either tungsten or aluminum (*claim 58*). However, with regard to (a): because Ikeda et al teach the memory array to comprise transistors (Q_t), the control circuit to comprise transistors (Q_d), and the flip-flop circuit as data storage and retrieval unit (input/output circuit) to comprise both drive and transfer transistors (cf. column 1, line 11-39), and because a replacement of the polysilicide gate 7 for Q_d by titanium silicide as implemented for gate 13 of the transfer transistors would improve the response time of said gate 7 through an increase in the electrical conductivity of said gate 7 (the examiner takes official notice that metal conducts better than polysilicon), it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the abovementioned extraneous limitation. With regard to (b) and (c): as shown by Xu et al it is especially advantageous in the case of high aspect ratio contact holes to fill them with aluminum (cf. column 10, lines 4-18) that subsequently forms a high-conductivity alloy (titanium-aluminum) (cf. column 26, lines 9-11) with the titanium material of a liner of the walls (except the silicided bottom) for the purpose of increasing the electrical conductivity (cf. column 10, lines 10-32) for reduced response time. Because response time it essential to the operational quality of memory devices motivation is established. Because the teaching of Xu et al only would require a different filling of the same contact hole the inventions are combinable. Because the aluminum sputtering process (cf. abstract, line 1) taught by Xu et al is especially designed for present-day high-aspect-ratio devices and is independent of all other steps in the making of the device as taught by Ikeda et al, success in combining the inventions can be reasonably expected.

Finally, the method used for producing the titanium layer is irrelevant to the present device type invention (*claim 59*).

8. ***Claims 47, 61, 65, and 69*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al (5,239,196). As detailed above, claims 60, 64, and 68 anticipated by Ikeda et al, while claim 46 is unpatentable over Ikeda et al. Ikeda et al do not necessarily teach the titanium alloy layer to include besides titanium also zinc. However, it is commonly understood in the art of ohmic contacts that the reason for inserting the titanium silicide is to arrange for a more gradual transition between the resistivity of the polysilicon semiconductor regions and the preferably highly conducting interconnect metal, for which aluminum is preferred. Zinc would therefore obviously be a suitable material to provide an intermediate layer in view of its resistivity, which is about a factor 3 higher than aluminum. Once zinc is used in the lower portion of the contact hole as a filling material, the alloy formed with titanium would necessarily also include zinc.

9. ***Claims 73, 78, and 82*** are rejected under 35 U.S.C. 103(0a) as being unpatentable over Ikeda et al (5,239,196) in view of Xu et al (6,217,721 B1). As detailed above, claims 72, 77, and 81 are unpatentable over Ikeda et al. Ikeda et al do not necessarily teach the titanium alloy layer to include besides titanium also zinc. However, it is commonly understood in the art of ohmic contacts that the reason for inserting the titanium silicide is to arrange for a more gradual transition between the resistivity of the polysilicon semiconductor regions and the preferably highly conducting interconnect metal, for which aluminum is preferred. Zinc would therefore obviously be a suitable

material to provide an intermediate layer in view of its resistivity, which is about a factor 3 higher than aluminum. Once zinc is used in the lower portion of the contact hole as a filling material, the alloy formed with titanium would necessarily also include zinc.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
May 28, 2002

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